

English Translation of JP61-140296**(19) Japanese Patent Office (JP)****(11) Publication Number: Sho 61-140296****(43) Date of publication of application: June 27, 1986****5 (12) Patent Laid-open Official Gazette (A)****(51) Int.Cl.⁴****H 04 N 9/12****G 02 F 1/133****G 09 G 3/36****10 The Number of Claims: 1 (6 pages in total)****Request of Examination: not made****(54) Title of the Invention: ELECTRONIC VIEWFINDER****(21) Application number: Sho 59-263362****(22) Date of filing: December 13, 1984****15 (71) Applicant: SEIKO EPSON CORP.****2-4-1 Nishi Shinjuku, Shinjuku-ku, Tokyo, Japan****(72) Inventor: Toshiyuki MISAWA****c/o Suwa Seikosha Co., Ltd.****3-3-5 Owa, Suwa, Nagano, Japan****20 (74) Representatives: Patent attorney:****Tsutomu MOGAMI****Specification****1. [Title of the Invention]****25 ELECTRONIC VIEWFINDER****2. [Scope of Claim]****1) An electronic viewfinder characterized by comprising:****a panel module composed of a liquid crystal panel and a driver circuit for said liquid crystal panel;****30 an integrated chrominance signal processing circuit;****JP61-140296**

an integrated timing signal generation circuit; and
an integrated interface circuit directly connected with said panel module to drive said panel module.

2) An electronic viewfinder set forth in claim 1 characterized in that:

5 said liquid crystal panel is an active matrix liquid crystal panel having a pixel matrix composed of a thin film transistor on an insulating substrate; and

said liquid crystal panel is formed by integrating a driver circuit composed of a thin film transistor on the same insulating substrate as said pixel matrix.

3. Detailed Description of the Invention

10 [Industrial Field for the Invention]

The present invention is related to an electronic viewfinder which employed a liquid crystal panel for image display, and said electronic viewfinder is applied to a household video camera and so forth.

[Prior Art]

15 Conventionally, a small size video monitor with a CRT (Cathode Ray Tube) for a viewfinder and so forth of a video camera has been developed and on the market. In the meantime, a monochrome small size video monitor has been showing good results so far. A full color small size video monitor, however, has not yet grown popular because of its complicated manufacturing method and a high cost for its performance.

20 FIGs. 6(a) and (b) show an example of the electronic viewfinder which is already developed and released. As shown in FIG. 6(a), a color picture tube consists of an electron gun 1, a shadow mask 2 and a fluorescent screen 3 and so forth.

Furthermore, a circuit block of the electronic viewfinder consists of a color demodulation circuit 4, a synchronous separator circuit 5, a vertical deflection circuit 6, a horizontal deflection
25 circuit 7, a high-pressure rectification circuit 8, and a picture tube 9 as shown in FIG. 6(b).

The prior art above is an example which adopted a shadow mask system, while an electronic viewfinder which adopted a CRT of a beam index system is described in detail in pages 28 to 36 of "Television Technique" of September 1983.

[Problems to be Solved by the Invention]

30 Specifications of the electronic viewfinder with a CRT which appeared in the aforesaid

document "Television Technique" of September 1983 are shown in table 1.

According to the table 1, a small size video monitor with a CRT is obviously too big and heavy to apply to a video camera as an option, especially to a handy-type video camera. Moreover, it consumes 2.7W, which is too much.

- 5 Also, if a shadow mask system is adopted, shadow mask holes have to be formed through etching a metal plate of $100\mu\text{m}$ to $200\mu\text{m}$ in thickness by photolithography. Therefore, a hole pitch can be no more than around $200\mu\text{m}$ at its biggest. A small size CRT hence has a limit in raising resolution.

System		Type II index 1/1 system Front-lighting system	Monochrome system
Cathode ray tube	Screen size	1.5 inch	1.5 inch
	Deflection	36°	36°
	Neck diameter	13 ϕ	13 ϕ
	Phosphor	129 sets	-
	Electron gun	H-UPF	BPF
	Beam spot diameter	$90\mu\text{m}\phi$	$160\mu\text{m}\phi$
	High voltage	7.5kV	4kV
	Length	129mm	108mm
Vertical resolution		more than 350 TV lines	270 TV lines
Power consumption		2.7W	1.7W
Size		W250 x L130 x H76	W57 x L194 x H52
Weight		700g	400g

Table 1

The present invention is intended to resolve the defects of the small size video monitor with a CRT as described above.

[Means for Solving the Problem]

- 15 To solve the defects described above, the electronic viewfinder is composed by using a panel module with a liquid crystal panel as a display and integrating a chrominance signal

processing circuit, a timing signal generation circuit and the interface circuits directly connected with said panel module to drive it. Also, an active matrix liquid crystal panel having a pixel matrix formed of thin film transistors (hereinafter referred to as TFT) is employed to said liquid crystal panel, and driver circuits using TFTs on the same substrate as this pixel array are
5 integrated.

[Operation]

By applying an active matrix liquid crystal panel of TFTs as a display to the electronic viewfinder, providing integrated driver circuits of TFTs on a TFT substrate of said active matrix liquid crystal panel and forming every major peripheral circuit constituting the electronic
10 viewfinder as an integrated circuit, the electronic viewfinder which is smaller, thinner, lighter, and consumes less power can be obtained. Moreover, a TFT substrate of an active matrix liquid crystal panel is manufactured through the same steps as an integrated circuit by photolithography, therefore, a pixel can be easily miniaturized down to $10\mu\text{m}$ pitch or so.

[Embodiments]

FIG 1 is a block diagram illustrating an embodiment of an electronic viewfinder of the present invention. In FIG 1, 10 is a chrominance signal processing circuit, 11 is a timing signal generation circuit, 12 is an interface circuit, 13 is an active matrix liquid crystal panel, 14 is a gate line driver (hereinafter referred to as Y driver), 15 is a data line driver (hereinafter referred to as X driver), 16 is a pixel matrix, and 17 is a backlight means. Said circuits 10, 11, and 12
20 are all integrated.

FIG 2 illustrates an example of a constitution that said active matrix liquid crystal panel 13 has a driver built-in. In FIG 2, 18 is a Y driver using TFTs, 19 and 20 are X drivers using TFTs, 21 is a pixel matrix using a TFT 22 and the like, 23 is a gate line, and 24 is a data line. The Y driver 18 consists of a shift register, the X drivers 19 and 20 consist of shift registers and
25 sample holders.

FIG 3 is a block diagram illustrating an example of a constitution of an interface circuit in FIG 1. In FIG 3, 25 and 26 have a function to convert a video signal to a signal for a liquid crystal panel, 25 is an alternating current reverse circuit, 26 is a combination circuit of R (red), G (green), and B (blue). 27, 28, and 29 have a function to convert a timing signal to a signal for
30 liquid crystal panel with a driver built-in, 27 is an X clock generation circuit to generate a clock

signal for X drivers, 28 is a level shifter for an X clock, and 29 is a level shifter for a Y clock.

Now, the operation of the present invention will be described.

A composite video signal 30 which is inputted into an electronic viewfinder module illustrated in FIG. 1 is demodulated into primary color signals of R, G, and B through the chrominance signal processing circuit 10, and then sent to the interface circuit 12. Meanwhile at the timing signal generation circuit, the composite video signal 30 is converted to a basic timing signal 32 which is minimum required to drive a liquid crystal image display device. 33 is a burst gate signal required for color demodulation.

Primary color signals 34, 35, and 36 which are transmitted from the chrominance processing circuit to the interface circuit shown in FIG. 3 as described in 37 of FIG. 4(a) are first converted through the alternating current reverse circuit 25 to such alternating reversed primary color signals 39, 40, and 41 for a liquid crystal display as shown in 38 of FIG. 4(a). T^{FRM} , T^{FLD} , and T^H in FIG. 4 respectively means 1 frame period, 1 field period, and 1 horizontal scanning period. A liquid crystal display is driven by the video signal like 38 which is reversed per field so that a liquid crystal member is not deteriorated and a flicker is prevented. Each primary color signal 39, 40, and 41 for driving liquid crystal is converted through the combination circuit 26 of R, G, and B to video signals 43, 44, and 45 of which the coloration is changed per 1 horizontal scanning period (hereinafter referred to as 1H) as shown in 42 of FIG. 4(a), and then provided to a liquid crystal panel. Like this, a liquid crystal panel is driven by changing coloration per 1H because the coloration of a color filter to set up in a liquid crystal panel is in mosaic as shown in FIG. 5 in order to raise the visible resolution. In FIG. 5, 46, 47, and 48 are video signal lines in the liquid crystal panel and said video signals 43, 44, and 45 are provided to them respectively. Said combination circuit of R, G, and B is not needed if a color filter set up in the liquid crystal panel is in stripe instead of the coloration shown in FIG. 5 or a monochrome liquid crystal panel is adopted.

Basic timing signals 49, 50, 51, and 52 which are transmitted from the timing generation circuit 11 to the interface circuit shown in FIG. 3 are converted to clock signals 53, 54, 55, 56, 57, 58, 59, and 60 for driving active matrix liquid crystal panel with a driver built-in. One such example is shown in FIGs. 4(b) and (c). 49 and 50 in FIG. 4 are basic timing signals which are transmitted from the timing generation circuit 11. 49 has information of 1 field period and 50

has information to determine 1 horizontal selection period. These signals are converted to the signals 58, 59 and 60 whose levels and amplitude are enough to drive a Y driver 18 using TFTs shown in FIG 2, and then provided to said Y driver 18. In the Y driver 18, the signal 58 is used as a start signal for a shift register, and the signals 59 and 60 are used as transfer clocks. Also, in FIG 4(c), 51 and 52 are basic timing signals transmitted from the timing generation circuit 11. The signal 51 has information to determine the location to start horizontal scanning, and the signal 52 has information to determine the timing and spacing to sample the video signals. In FIG 4(c), T^H shows 1 horizontal scanning period and a sampling spacing of video signals. The signals 51 and 52 are converted to signals 61, 62 and 63 which have timing information to drive X drivers 19 and 20 using TFT in FIG 2 at the X clock generation circuit 27. After that, they are converted to the signals 53, 54, 55, 56 and 57 whose levels and amplitude are enough to drive said X drivers 19 and 20 by the level shifter 28, and provided to a panel with a driver built-in. The signal 53 is used as a start signal for shift registers of X drivers 19 and 20, the signals 54 and 55 are used as transfer clocks for a shift register of the X driver 19, and the signals 56 and 57 are used as transfer clocks for a shift register of the X driver 20.

As a TFT constituting an active matrix panel is formed with polycrystalline silicon or amorphous silicon and the like, its quality is inferior compared with MOSFET, especially in the respect that ON resistance is high. Because of this, a driver consisting of TFTs might have the following inconveniences: (1)The frequency to operate the shift register is low, (2)It is impossible to drive a big load capacitance with TFT, e.g. a clock line, (3)The necessary power voltage is high compared with a general logic IC. To solve these TFT-specific problems, the present invention takes the following means and the like: (1)Provide shift registers in a plurality of lines as shown in FIG 2, (2)Provide an integrated interface circuit to drive a panel with a driver built-in, to provide all transfer clock signals of a shift register using TFTs from said interface circuit.

FIG 4(d) illustrates an example of the relation of a voltage level and an amplitude of a timing signal 64 generated by a timing signal generation circuit 11, a video signal 65 alternating reversed by the alternating current reverse circuit 25, and a signal 66 to drive the drivers 18, 19 and 20 using TFTs. All signal processing circuits in FIG 1 operate at a voltage of less or equal to the operating voltage V_0 of a panel 13 with a driver built-in. The V_0 is less or equal to 30V.

[Effect]

An electronic viewfinder of the present invention has 2 integrated signal processing circuits, which are a chrominance signal processing circuit and a timing signal generation circuit, and an interface integrated circuit for driving a panel, and an active matrix panel with a driver built-in as major constituents to make the electronic viewfinder remarkably smaller, thinner, and lighter. Furthermore, as said timing signal generation circuit and the interface circuit for driving a panel can be made with CMOS and so can a TFT driver, it is not difficult to lower the power consumption to less than 1W, even if the power consumption of a backlight is added. Moreover, adding to the integrated peripheral circuits, an active matrix substrate with a driver built-in makes the components extremely fewer, which leads to a remarkable cost reduction.

As an active matrix liquid crystal panel is used to an image display, a pixel can be miniaturized to $10\mu\text{m}$ pitch in the ultimate sense, so that the resolution is raised to improve the performance as a viewfinder such as focusing. Additionally, a display with less distortion than CRT is obtained as an image is reproduced by a matrix system.

According to the present invention, considerable effect as described above is brought about.

4. [Brief Description of the Drawings]

FIG 1 is a block diagram to describe an embodiment of the present invention.

FIGs. 2 and 3 are diagrams to describe the constituents in FIG 1 in more detail.

FIGs. 4(a), (b), (c) and (d) are diagrams to describe the operation of the embodiment of the present invention.

FIG 5 is a diagram to describe the operation as well.

FIGs. 6(a) and (b) are diagrams to describe the prior art.

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